

## IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

reading a design description for a heterogeneous reconfigurable device that includes a plurality of programmable elements with different underlying architectures, wherein a first type of the plurality of programmable elements is capable of executing instructions, and a second type of the plurality of programmable elements is capable of different configurations to implement logic, the design description including a plurality of functions to map to the plurality of programmable elements;

combining the plurality of functions within the design description into groups based at least in part on possible programmable element types upon which the plurality of functions could successfully map; and

estimating power consumption of the groups using a pre-determined database that estimates the power for each instruction or configuration, depending on the underlying architecture of a target programmable element type for each group; and

analyzing the groups for compliance with user-specified constraints, wherein the user-specified constraints include power consumption constraints.

2. (Canceled)

3. (Currently Amended) The method of claim 1 wherein analyzing comprises further comprising estimating area occupied by the groups.

4. (Currently Amended) The method of claim 1 further comprising re-combining the plurality of functions into groups, re-estimating power consumption, and re-analyzing the groups for compliance with the user-specified constraints.

5. (Original) The method of claim 1 wherein analyzing comprises comparing estimated parameters with prioritized user-specified constraints.
6. (Original) The method of claim 1 further comprising compiling the functions to run on processing elements within the heterogeneous reconfigurable device.
7. (Original) The method of claim 6 further comprising placement of the groups onto particular processing elements within the heterogeneous reconfigurable device.
8. (Original) The method of claim 7 further comprising analyzing the placement for compliance with user-specified constraints.
9. (Currently Amended) The method of claim 8 ~~wherein analyzing the placement comprises further comprising~~ estimating latency.
10. (Original) The method of claim 9 wherein estimating latency comprises estimating interconnect delay.
11. (Original) The method of claim 9 wherein estimating latency comprises estimating processing latency.
12. (Original) The method of claim 9 wherein estimating latency further comprises estimating processing latency and interconnect latency.
13. (Original) The method of claim 7 further comprising producing a file with a placed design for profiling.
14. (Original) The method of claim 13 further comprising profiling the design and comparing with user-specified constraints.

15. (Currently Amended) The method of claim 14 further comprising the plurality of functions in response to the profiling.

16. (Original) The method of claim 14 further comprising re-performing placement in response to the profiling.

17. (Currently Amended) A method comprising:

mapping a plurality of functions into groups;  
placing the groups on resources within a heterogeneous reconfigurable device; the resources including a plurality of programmable elements with different underlying architectures, wherein a first type of the plurality of programmable elements is capable of executing instructions, and a second type of the plurality of programmable elements is capable of different configurations to implement logic;

estimating power consumption of the groups using a pre-determined database that estimates the power for each instruction or configuration, depending on the underlying architecture of a target programmable element type for each group;

analyzing the groups for compliance with user-specified constraints, wherein the user-specified constraints include power consumption constraints;

producing a mapped and placed design representation;

profiling the design representation; and

comparing results from the profiling with the user-specified constraints.

18. (Original) The method of claim 17 further comprising re-mapping the plurality of functions into groups.

19. (Original) The method of claim 17 further comprising re-placing the groups on resources.

20. (Original) The method of claim 17 wherein comparing results comprises comparing an estimated latency with a latency specified in the user-specified constraints.

21. (Original) The method of claim 20 wherein the estimated latency includes processing latency and interconnect latency.

22. (Original) The method of claim 17 wherein the user-specified constraints include latency, power, and throughput.

23. (Currently Amended) An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine performing:

reading a design description for a heterogeneous reconfigurable device that includes a plurality of programmable elements with different underlying architectures, wherein a first type of the plurality of programmable elements is capable of executing instructions, and a second type of the plurality of programmable elements is capable of different configurations to implement logic, the design description including a plurality of functions to map to the plurality of programmable elements;

combining the plurality of functions within the design description into groups based at least in part on possible programmable element types upon which the plurality of functions could successfully map; and

estimating power consumption of the groups using a pre-determined database that estimates the power for each instruction or configuration, depending on the underlying architecture of a target programmable element type for each group; and

analyzing the groups for compliance with user-specified constraints, wherein the user-specified constraints include power consumption constraints.

24. (Currently Amended) The apparatus of claim 23 wherein the machine-accessible instructions when accessed further result in the machine performing:

re-combining the plurality of functions into groups; and

re-analyzing the groups for compliance with the user-specified constraints.

25. (Original) The apparatus of claim 23 wherein the machine-accessible instructions when accessed further result in the machine performing:

compiling the functions to run on processing elements within the heterogeneous reconfigurable device.

26. (Original) The apparatus of claim 23 wherein analyzing comprises comparing estimated parameters with prioritized user-specified constraints.

27. (Currently Amended) An electronic system comprising:

a processor; and  
a static random access memory to hold instructions that when accessed result in the processor performing reading a design description for a heterogeneous reconfigurable device[[],]  
that includes a plurality of programmable elements with different underlying architectures,  
wherein a first type of the plurality of programmable elements is capable of executing  
instructions, and a second type of the plurality of programmable elements is capable of different  
configurations to implement logic, the design description including a plurality of functions to  
map to the plurality of programmable elements; combining the plurality of functions within the  
design description into groups[[],] based at least in part on possible programmable element types  
upon which the plurality of functions could successfully map; estimating power consumption of  
the groups using a pre-determined database that estimates the power for each instruction or  
configuration, depending on the underlying architecture of a target programmable element type  
for each group; and analyzing the groups for compliance with user-specified constraints wherein  
the user-specified constraints include power consumption constraints.

28. (Currently Amended) The electronic system of claim 27 wherein the instructions when accessed further result in the processor performing re-combining the plurality of functions into groups, and re-analyzing the groups for compliance with the user-specified constraints.

29. (Original) The electronic system of claim 28 wherein analyzing comprises comparing estimated parameters with prioritized user-specified constraints.